In re Patent Application of:
PEZZINI
Serial No. **10/634,150**
Filing Date: **AUGUST 4, 2003**

REMARKS

The Examiner is thanked for the thorough examination of the present application. In view of the arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a serial peripheral interface. As recited in independent Claim 5, for example, the serial peripheral interface includes a memory coupled to at least one data bus and an address bus. The memory is for storing data from the at least one data bus associated with a plurality of peripheral devices based upon respective data addresses on the address bus, and the memory has a respective transmit data section and a respective receive data section for each peripheral device. In addition, the memory also has a configuration command section for storing configuration commands for use in communicating with each of the peripheral devices. The serial peripheral interface further includes a data pointer for pointing to transmit and receive data section addresses, and a control register for controlling the data pointer based upon at least one configuration command associated with a selected peripheral device. Moreover, the serial peripheral interface also includes a data transfer circuit for serially transferring data between the memory and the selected peripheral device based upon the at least one configuration command, and a configuration pointer for pointing to an address at which the at least one

configuration command is stored in the configuration command section based upon a data address on the at least one data bus.

Independent Claim 9 is directed to a related serial communication device, and independent Claim 13 is directed to a related serial data transfer method. Each of these claims recites pointing to (or determining) an address at which at least one configuration command is stored in a configuration command section of a memory based upon a data address on at least one data bus, similar to Claim 5.

II. The Claims Are Patentable

The Examiner rejected independent Claims 5, 9, and 13 over the prior art illustrated in FIGS. 1 and 2 of the application and discussed in the background (the "admitted prior art"), in view of U.S. Patent Publication No. 2004/0019726 to Kelley et al. The Examiner correctly acknowledges that the admitted prior art fails to teach or fairly suggest a configuration pointer for pointing to an address at which the at least one configuration command is stored in the configuration command section of the memory based upon a data address on the at least one data bus, as recited in the above noted independent claims. However, the Examiner contends that Kelley et al. provides this noted deficiency. Kelley et al. is directed to a buffer management and transaction control method for serial I/O systems. In particular, the Examiner points to paragraph 0034 of this reference which describes a "link list of tasks" for tracking outstanding work tasks as support for this contention.

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It is respectfully submitted that the Examiner mischaracterizes the teachings of Kelley et al., and thus when considered as a whole the proposed combination of references fails to teach all of the claimed recitations. In particular, in the Kelley et al. system a device driver stores a linked list of outstanding work tasks to be completed by a device driver in a system memory. Whenever the device driver updates the task list in the system memory, the device driver accesses the device to indicate that an updated task list is available. The device then picks up new work tasks to be handled by checking the task list in the system memory, and it posts an interrupt to indicate which task(s) has been completed. The device driver then updates the linked list in the system memory. See paragraphs 0034-0035 of Kelley et al.

As an initial matter, the linked list of work tasks of the Kelley et al. system does not point to an address at which one or more configuration commands for a serial interface device are stored in a configuration section of a memory. As noted above, the Kelley et al. link pointers point to work tasks to be performed by a given device in an order assigned by the device driver.

Moreover, the Kelley et al. linked list of tasks does not provide a pointer to a configuration command(s) stored in a command section of a memory based upon a data address on at least one data bus. As noted above, in the Kelley et al. system the device driver pre-determines the order in which tasks are to be performed and stores this information in the linked list. The

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linked list pointer points to a next task to be performed based upon an order set by the device driver that is stored in the system memory, not an address on a data bus, as noted above.

Accordingly, since the remaining prior art of record fails to teach or fairly suggest the above-noted deficiencies, it is submitted that independent Claims 5, 9, and 13 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,

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